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## PATENT ABSTRACTS OF JAPAN

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**H01L 29/78****H01L 21/265****H01L 29/60**(21) Application number: **60067811**(22) Date of filing: **30.03.85**(71) Applicant: **TOSHIBA CORP**(72) Inventor: **YOSHIDA MASAYUKI****(54) MANUFACTURE OF MOS TYPE SEMICONDUCTOR DEVICE****(57) Abstract:**

**PURPOSE:** To prevent a short channel effect by providing a process by which a gate electrode is formed, a process by which a reverse conduction type impurity diffusion region is shaped, a process by which a deep one conductivity type impurity diffusion region is formed, and a process by which a reverse conductivity type high-concentration impurity diffusion region is shaped.

**CONSTITUTION:** An inter-element isolation oxide film 12 and a gate oxide film 13 are formed to a P-type silicon substrate 11, polycrystalline silicon is deposited, and phosphorus ions are implanted, diffused and patterned to acquire a gate electrode 14. The gate oxide film 13 is removed while using the gate electrode 14 as a mask, an silicon oxide film 15 and an silicon oxide film 16 are shaped, and indentation sections 17 are obtained through RIE. Phosphorus ions are implanted while employing the gate 14 and the field oxide film 12 as masks to shape N regions 18. B ions are implanted slantingly to form P regions 19a, 19b in a shape that the regions 19a, 19b surround the whole side surfaces and lower surfaces of the N regions 18, a photo-resist 20 is patterned and shaped around the gate 14, and arsenic ions are implanted in high concentration while using the

photo-resist 20 as a mask to form N<sup>+</sup> regions 21. Accordingly, a punch-through and a short channel effect can be inhibited.

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